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09/757,273	01/10/2001	Tamer Yunten		6245

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/757,273	Applicant(s) YUNTEN, TAMER	
	Examiner Daniel Pan	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/10/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-24 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,5,7,8,9,11, 13 are rejected under 35 U.S.C. 102(a) (b) as being anticipated by Chul (4,964,803) .

3. As to claim 1, Chul disclosed a 4-bit teaching computer comprising at least :

a) central memory section (see fig.1 MEM, fig.2g , col.5, lines 25-31);

b) central processing unit (see fig.2b, see CPU in col.4, lines 55-60);

c) I/O section allowing manual programming of the computer (e.g. see the keyboard for entering the HEXA signal and the display in fig.1, see col.3, lines 29-36, col.5, lines 63-68, col.6, lines 1-47).

4. As to claim 2, Chul also included basic machine instructions (e.g. see fig.18 Add, Move, LDA, and Store).

5. As to claim 3, Chul also included emitting diode (e.g. see LED in col.3, lines 37-39).

6. As to claim 5, Chul also included Add function and no other arithmetic functions (see the Add function in fig.18).

7. As to claim 7, Chul also included a sum register (see the accumulator in col.9, lines 14-17).

8. As to claim 8, Chul also included clock and instruction fetch (e.g. see fetch cycle and clock in col.9, lines 1-13).

9. As to claim 9, Chul also included 2 4-bit registers (e.g. see each bit 4 bits in fig.2b [Acc][TR], see also col.13, lines 26-29, see also fig.16 for 4 bit bus format).

10. As to claim 11, Chul also included timing generation and decoder , counter (e.g. see the clock generation and counter in col.3, lines 27-29, col.5, lines 45-59, fig.2h, see the decoder in col.3, lines 54-55).

11. As to claim 13, Chul also included at least two registers with output buffer (e.g. see the 4 bit each output digital display in fig.2a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 4,14,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chul (4,964,803) in view of Lahti (4,722,049).

13. As to claims 2,4,14,15, , limitations of parent claim have been discussed in paragraph # 2,3, therefore, it will not be repeated herein Chul did not specifically show

his memory was a RAM for storing the instructions as claimed. However, Lahti disclosed a RAM for storing instructions (fig.10 G [402 RAM, col.10, lines 15-47). It would have been obvious to one of ordinary skill in the art to use Lahti in Chul for including RAM for storing instructions as claimed because the use of Lahti could provide Chul the ability to access the instructions at random read and write modes, therefore, increasing the accessibility and modifications of the instructions at any given time, and it could be readily achieved by predefining the RAM of Lahti into Chul such that the RAM memory for storing instructions could be recognized by Chul, and I doing so, provided a motivation.

14. Claims 10,16-19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chul in view of Grundy et al. (5,224,055).

15. As to claims 10, 16, limitations of parent claim have been discussed in paragraph # 2,3, therefore, it will not be repeated herein. Chul did not specifically show the breadboard as claimed. However, Chul did show circuit board including plurality of circuit sections (fig.1). In addition to Chul, Grundy disclosed a plurality of breadboards [106] (see the plug boards 106 in col.5, lines 52-68). It would have been obvious to one of ordinary skill in the art use Grundy for including the breadboards as claimed because the use of Grundy could provide Chul the capability of the circuit components of the microcomputer to be reconfigurable and tested ahead based on the specific requirement of the user, and because Chul was directed to the computer operations for teaching purpose (see col.1, lines 6-14), it would have been highly desirable to use the breadboards for the specific circuit board sections of Chul to

enhance the flexibility of the connections of the microcomputer's components to accomplish the teaching goal , and in doing so, provided a motivation.

16. Chul did not specifically show the number of the bread boards as 4 as claimed. However, Since no advantage of using the 4 breadboards compared to other number of bread boards can be found in the specification and in the claim, It is assumed the specific number of breadboard is not a required element which would change the scope of the invention. Therefore, it would have been obvious to one of ordinary skill in the art to use specific number of bread board, such as 4, as claimed because the specific number of bread boards is directed the number of the circuit boards or sections interconnected, and would not have changed the operation of the teaching computer. Unless applicant can show the unique advantages of using 4 bread boards instead of other number of bread boards, one of ordinary skill in the art should be able to recognize any specific number of bread boards could be used in the teaching computer.

17. As to claim 17, Chul' also included a timing generator inn a first section (see the circuit section of CG in fig.1, see the detailed structure of the circuit section in fig.2h).

18. As to claim 18, Chul also included program counter and arithmetic unit in a second section (see the circuit section of PC and ALU in fig.1).

19. As to claim 19, Chul also included two data registers [latch] and a bus consisting of 4 parallel conductors (4 bits) for interchanging data (see fig.16).

20. As to claim 21, Chul's control generator also located in second [PC] , third, [BR] and fourth [CR] sections (see the circuit sections [PC][BR][CR] in fig.1).

21. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chul in view of Grundy et al. (5,224,055) as applied to claim16-19 above, and further in view of Lahti (4,722,049).

22.

23. As to claim 20, neither Chul nor Grundy disclosed the RAM for storing the instructions as claimed. However, Lahti disclosed a RAM for storing instructions (fig.10 G [402 RAM, col.10, lines 15-47). It would have been obvious to one of ordinary skill in the art to use Lahti in Chul for including RAM for storing instructions as claimed for the reasons set forth in the paragraph # 13 above, and will not be repeated herein.

24. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chul (4,964,803) view of Grundy et al. (5,224,055) and Leeds et al. (4,709,971)

25. As to claims 22-24, Chul taught at least sets of chips for constructing central processing unit, I/O and memory [MEM] (see fig.1).

26. Chul did not specifically show the 4 breadboards as claimed. However, Grundy disclosed a plurality of breadboards (see the plug boards 106 in col.5, lines 52-68). One of ordinary skill in the art should be able to recognize any specific number of bread boards could be used in the teaching computer. For the reasoning, see paragraph #1 above.

27. As to the power strip, neither Chul nor Grundy specifically show the power strips as claimed. However, Leeds showed a strip for activating a CPU unit (e.g. see col.7, lines 27-37). It would have been obvious to one of ordinary skill in the art to use Leeds in Chul and Grundy for including the power strip as claimed because the use of Grundy could provide Chul and Grundy the protected transfer of the power supply on the board, thereby eliminating the unnecessary power dissipations due to the circuit overheads, and because Grundy also showed his breadboards (plug boards) including a power supply with ground ports (e.g. see col.5, lines 9-11, see also the power rails [122] in col.6, lines 25-34, see fig.8 122), which was an indication of the concern of the power dissipation, and therefore, the need of using a power protection circuit , such as a power strip , in order to reduce the excessive power, and in doing so, provided a motivation.

28. Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Chul (4,964,803) in view of Yamada et al. (5,424,969).

29. As to claim 12, Chul did not specifically show the AND and OR gates in the timing generator as claimed. However, Yamada disclosed a timing generator for synchronizing the clock signals including a AND and OR gates (e.g. see fig.14, see col.20, lines 66-68, col.21, lines 1-40 , see AND and NOR with NOT for OR). It would have been obvious to one of ordinary skill in the art to use Yamada to include the AND and OR gates as claimed because the use of Yamada could provide Chul the ability of generating the predetermined timing signals based on the a specific block of the logic circuit, thereby increasing the adaptability of the timing generating circuit, and because although the logic block of Chul's timing generation was not explicitly shown, and since no specific typo of AND and OR gates is being recited in the claim, one of ordinary skill in the art should be able to recognize the applicability of standard logic gates, such as the AND and OR , which had been widely used in the field at the time the claimed invention was made, into Chul's timing generating circuit to generate the timing signals based on the logic gates, and the examiner believes that one of ordinary skill in the art should be able to recognize the applicability of logic gates AND, OR etc. into the timing generation unless the AND and OR have specific and unique connection and logic structure, and therefore, for the above reasons, provided a motivation.

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Marui is cited for the basic teaching of the breadboard for testing (e.g. see fig.1, col.10, lines 10-63, see also col.2, lines 37-46);

b) Lewis (4,517,671) is cited for the teaching of the teaching of the dispalyable computer operations (e.g. see fig.2).

c) Cannon et al (Designing with Microprocessors Lesson Summaries) is cited for the basic teaching of the 4 bit slice processor (see pages 72,73).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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